Deliverable D5.1

Demonstrator definitions

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Project Acronym	**FirstTo6G**
Project Title	**Fourier-Domain TRx solutions enabling widespread realisation of 6G**
Project No.	**101139167**
Topic	**HORIZON-JU-SNS-2023-STREAM-B-01-05**
Project start date	**1 January 2024**
Nature	**Report**
Dissemination level	**Public**
Due date	**M08**
Date of delivery	**M16**
Date of resubmission	**M18**
Lead partner	**RWTH**
Contributing partners	**InCirT, RWTH**
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Co-funded by the European Union

Project funded by
Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra
Swiss Confederation

This work was supported by the FirstTo6G project, which has received funding from the Smart Networks and Services Joint Undertaking (SNS JU) and its members under the European Union's Horizon Europe programme and by the Swiss State Secretariat for Education, Research and Innovation (SERI).

Revision History

Version	Date	Author	Comment
0.1	09.09.2024	Renato Negra	First draft, structure and content outline
0.2	28.09.2024	Erkan Bayram, Mohamed Elsayed	Added contributions in various sections
0.3	27.02.2025	Renato Negra	Merging of two documents
0.8	03.03.2025	Renato Negra, Erkan Bayram	Review and final draft content addition
0.9	26.03.2025	Renato Negra	Revisions
0.9.1	31.03.2025	Oner Hanay	Review and final additions
	04.04.2025	Johanna Hanning	Review
0.9.9	08.04.2025	Renato Negra	Revisions
1.0	08.04.2025	Peter Ulrich	Final version, approved by the coordinator
1.1	25.06.2025	Renato Negra	Revisions
2.0	27.06.2025	Peter Ulrich	Final version, approved by the coordinator
2.1	08.07.2025	Renato Negra	Revisions according to Reviewers comments

Contents

Abbreviations, participant short names

Abbreviations

ADC	Analogue Digital Converter
AFE	Analogue Frontend
AI	Artificial intelligence
APSK	Amplitude Phase-shift Keying
AR	Augmented Reality
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Coplanar Waveguide
DAC	Digital Analogue Converter
DSP	Digital Signal Processing
EVM	Error Vector Magnitude
FDADC	Fourier Domain ADC
FDDAC	Fourier Domain DAC
FDSOI	Fully Depleted Silicon-on-Insulator
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FWA	Fixed Wireless Access
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GEO	Geostationary Earth Orbit
GUI	Graphical User Interface
IC	Integrated Circuit
iFFT	Inverse Fast Fourier Transform
IF-VG	Intermediate Frequency Variable Gain Amplifier
InP	Indium Phosphide
IoT	Internet of Things
LEO	Low Earth Orbit
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Lowpass Filter
MEO	Medium Earth Orbit
MIMO	Multiple Input Multiple Output
ML	Machine Learning
PA	Power Amplifier
PCB	Printed Circuit Board
PMU	Power Management Unit

QAM	**Quadrature Amplitude Modulation**
R&D	**Research and Development**
RFIC	**Radio-Frequency Integrated Circuit**
Rx	**Receiver**
SiGe	**Silicon Germanium**
TRx	**Transceiver**
TDD	**Time Division Duplexing**
URLLC	**Ultrareliable Low-Latency Communications**
V2X	**Vehicle-to-Everything**
VGA	**Variable Gain Amplifier**
VR	**Virtual Reality**
XR	**Extended Reality**

Participant short names

ArgoSemi	**Argo Semiconductors SA**
InCirT	**InCirT GmbH**
SCIPROM	**SCIPROM Sàrl**
SIVERS	**Sivers Wireless AB**
RWTH	**Rheinisch-Westfälische Technische Hochschule Aachen**
YEDITEPE	**Yeditepe University**

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Summary

This deliverable presents the FirstTo6G demonstrators, *i.e.*, two demonstrators used in the FirstTo6G project to participate in exhibitions and demo events, as well as to provide vertical sectors with a 6G reference platform for testing. The main content of the document refers to the description of the specification and design activities conducted during the period up to M15 of the project, conversely to the original M8. As explained in the document, the development of the two FirstTo6G demonstrators aims for a compact physical layout to ensure portability and ease of setup. However, whereas the below-100-GHz (V-band) hardware demonstrator aims to develop an almost monolithic approach, the above-100-GHz (D-band) demonstrator integrates building blocks from different technologies. Moreover, the modular way of the D-band demonstrator which includes the V-band chipset and extending it for operation in the 140-170 GHz band, enhances the variety of test cases and experiments that the FirstTo6G demonstrators can support. All activities reported in this document abide by the need to meet a major objective of the project, *i.e.* the realisation of versatile broadband demonstrators for application in a variety of different 6G scenarios.

As stated in the project application, the two demonstrators aim to show and verify the relevant performance for application in future 6G systems. Since to date, no specific future 6G application is well defined, the approach of demonstrating the suitability of the developed hardware for a large variety of potential 6G applications, this document aims at collecting the common requirements for future applications from different sources to then derive the common electrical properties of as many envisioned 6G systems as possible. This research has led to the definition of the **main performance parameters** for which the two demonstrators are going to be tested.

High transmission data rates of 56 Gbps or higher (competing with photonic systems) while using **high bandwidths** (8 GHz in V-band and up to 16 GHz in D-band) with **different broadband modulation schemes** (128QAM in order to comply with IEEE 802.11ay) to achieve **spectral efficiency** defines the main goals of the project. The developed 6G system demonstrators shall be able to increase the data rate by adopting both **MIMO techniques** and the transmission in two **different noncontiguous frequency bands**, which will also allow for **enhanced connectivity** options such as **signal robustness, ultralow latency, channel bonding, reliability, frequency agility**. These features will be enabled by the **adaptive antenna array systems** to be developed within the project and shall be demonstrated in measurements. Additional linearisation might be required to meet the **signal quality** requirements for high data-rate transmission as well as **energy and regulatory spectral efficiency**.

Sustainability will be demonstrated by testing the capability of **dynamic power scaling** and by the approach-inherent **reduced signal processing speed** for the wide instantaneous modulation bandwidths compared to canonical and competing systems. In addition, dynamic power scaling will be also demonstrated through the capability of using **different instantaneous modulation bandwidths**, which together with varying complex modulation schemes demonstrates the **software-defined radio capabilities** of the developed hardware. Moreover, these features shall also be demonstrated by showcasing the possibility of implementing **joint communication and sensing applications**.

Additional project targets such as the **high level of integration, price competitiveness, and scaling** will not be tested, as they are implicit by the **use of Si-based technologies** for most of the transceiver blocks. **Multiple AFE functionalities** will be implemented in the high-performance 22nm FDSOI technology. This will also result in a **small form factor and price competitiveness** of a future product based on the research outcomes.

Finally, the accuracy of the proposed **system-level modelling methodology and link-budget calculation** approach using Cadence Virtuoso will be tested by comparing measurement results with simulations.

By verifying these parameters, the aim of the project to demonstrate the feasibility of the proposed TRx solutions for large-scale deployment in future diverse environments and 6G applications shall be achieved.

1. Introduction

As the demand for faster and more reliable wireless communication intensifies, the development of sixth-generation (6G) networks has become crucial. The FirstTo6G project is committed to leading the way in advanced transceiver solutions by utilizing Fourier-Domain techniques to achieve the stringent performance requirements of 6G technology. This initiative is focused on overcoming the key challenges of high-frequency communication, particularly targeting frequencies in the D-Band and those in the millimetre-wave frequency range below 100 GHz.

1.1 Project objectives

The primary objective of the FirstTo6G project is to develop and validate innovative transceiver (TRx) solutions that will drive the widespread adoption of 6G technology. Specific goals include:

- **High-Frequency TRx Design:** Developing transceiver components that can operate efficiently and effectively in the millimetre-wave sub-100 GHz frequency range, which is crucial for 6G communication.
- **Fourier-Domain Techniques:** Implementing Fourier-Domain methodologies to enhance signal processing, improve spectral efficiency, and reduce latency.
- **System Integration:** Ensuring seamless integration of analogue and digital components to maintain signal integrity and overall system performance.
- **Feasibility and Scalability:** Demonstrating the feasibility of the proposed TRx solutions for large-scale deployment in diverse environments and for a large variety of future applications.

1.2 Scope of the deliverable: Demonstrator definitions

This document is dedicated to the work performed for the realization of the FirstTo6G hardware demonstrators. The document serves as a reference point for the current status of the conducted integration activities, as well as a comprehensive descriptor of the functional components of the demonstrators. We note that the work reported in this document is linked to the activities of WP6 of the project (especially the dissemination and demonstration tasks) and as such, it can complement any participation in related events.

The scope of this deliverable is hence to report on the setup planned to demonstrate the capabilities of the two demonstrators, *i.e.* the below- and above-100-GHz transceivers. This is done by defining the possible application scenarios, deriving common hardware requirements for these scenarios, and test cases to verify with measurements the fulfillment of these specifications.

For the V-band solution, the overall objective will be to develop an integrated digital-to-analogue converter (DAC) / analogue-to-digital converter (ADC) plus frontend (together 'TRx') demonstrator that achieves 6G performance with a focus on high energy efficiency, low cost, and security. The project goal is to achieve a modulation bandwidth of 8 GHz for the frequency range from 57-71 GHz and a very low energy consumption of only 26 pJ/bit transmitted including the complete data conversion, digital signal processing, and the frontend as well as clock generation. It will be integrated into a single chip in the commercial GF 22FDX technology, which will make it a) low-cost and b) highly secure.

The D-band solution of the project aims to the highest possible transmission data rate by exploiting the large contiguous bandwidths available in the D-band. Ideally, the use of up to 16 GHz of coherent bandwidth with higher-order modulation schemes shall be demonstrated. The complete transceiver demonstrator will consist of the 22nm FDSOI RFICs of the V-band solution in combination with dedicated up- and down-converting frontend modules (FEMs) in Silicon Germanium and III-V technologies which extend the operation frequency range of the 6G demonstrator to D-band. In this way, modular and flexible 6G hardware will be available at the end of the project.

1.3 Key outcomes

- Understanding what is technically possible to enable extremely high data-rate communication for 6G telecommunication in the millimetre-wave frequency range.

- Functioning hardware demonstrators which prove that 8 GHz and 16 GHz bandwidth systems for above and below 100 GHz can be implemented in an energy- and cost-efficient way.
- Demonstrate the key requirements for various possible future 6G transceiver systems based on realised hardware demonstrators.
- Portable and easy-to-set 6G demonstrator platforms

2. Background and available systems

2.1 Motivation for 6G transceivers

The global average mobile data usage per smartphone is projected to grow by over 20% annually for at least the next five years. To manage higher data rates within the constraints of radio frequency (RF) communication, two main strategies can be employed: A) improving the efficiency of existing channel bandwidth through higher modulation orders, or B) utilizing a broader portion of the RF spectrum by allocating wider bandwidth per connection. Achieving higher modulation orders requires improved signal quality, but physical limitations make further improvements in signal quality costly, as it demands exponentially increasing power consumption.

As a result, the focus has shifted to using more of the available RF spectrum. However, the spectrum below 57 GHz is crowded with various services, leaving insufficient bandwidth for ultrahigh-speed data communication, such as that expected with 6G. One promising frequency range for 6G is the D-band (110–170 GHz), with 130–175 GHz being particularly suitable for communication purposes. As shown in Figure 1, above 100 GHz there are multiple frequency bands with 2–12.5 GHz bandwidths that can support mobile and fixed wireless communications.

However, at these higher frequencies, signal propagation diminishes, necessitating more base stations to maintain a cohesive network. Therefore, unlicensed spectrum below 100 GHz, particularly in the V-band (40–75 GHz), should also be considered for enhanced range and capacity. The 57 GHz – 66/71 GHz frequency range offers up to 14 GHz of unlicensed spectrum, depending on regional regulations, and is being targeted by standards such as IEEE 802.11ad/ay and 3GPP Rel. 17 NR-U (unlicensed 5G). Given its low current usage and wide bandwidth, it is a potential candidate for 6G applications, with results possibly applicable to adjacent millimetre-wave bands like the E-band (60–90 GHz) and W-band (75–110 GHz).

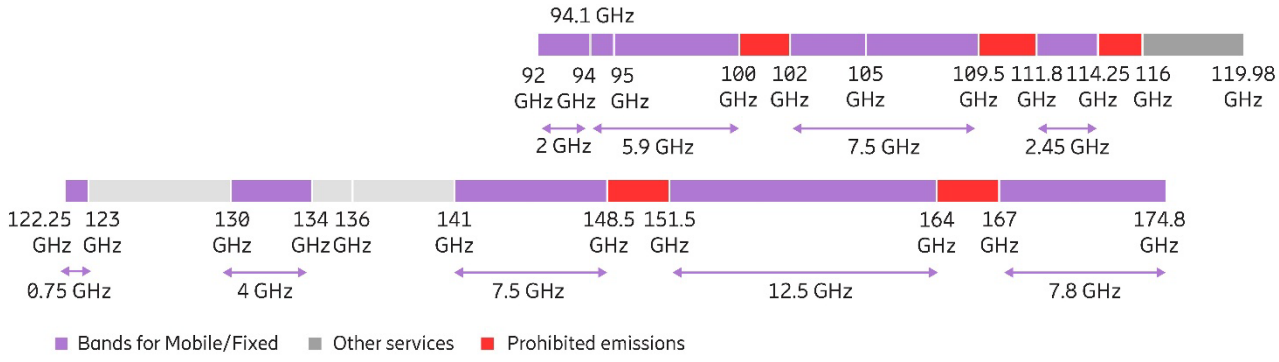

Figure 1. Frequency bands that are currently discussed for wide bandwidth 6G mobile communication (Source: https://www.ericsson.com/en/blog/2022/6/6g-spectrum-why-its-fundamental)

For 6G communication technology to become widely adopted, the hardware must meet several key criteria:

- Performance: The hardware must deliver wide modulation bandwidth at the necessary frequencies with sufficient signal quality to handle the high data rates expected in 6G.
- Energy Efficiency: It must operate efficiently to keep network infrastructure costs manageable, particularly in terms of electricity consumption, and ensure long battery life for mobile devices.

- Form Factor: The technology needs to be compact enough to be implemented in both base stations and mobile devices without compromising performance.
- Affordability: The semiconductor technology used must be cost-effective to enable mass adoption of 6G networks and devices.
- Security: The hardware must address potential security vulnerabilities to ensure the safety and privacy of communication networks.

These factors are essential to support the high performance, energy demands, and cost considerations required for a global 6G rollout.

2.2 Objectives of the demonstrator definitions

For V-band and D-band solutions, demonstrators target specific objectives which can be listed as follows:

- For the V-band, the objective is to integrate the developed 8-GHz DAC/ADC and the 57-71 GHz frontend onto a single chip, which will then be assembled into a module featuring an antenna on a printed circuit board (PCB). This setup will be used to evaluate the overall system performance which can be listed as follows:
  - **Validate high data rate transmission**: By operating in the V-band, the demonstrators can leverage wide unlicensed bandwidth to achieve data rates suitable for 6G, more specifically up to 56 Gb/s in this project.
  - **Evaluate spectral efficiency**: Demonstrators test new modulation schemes and waveform technologies that enhance spectral efficiency, enabling the transmission of more data within the same bandwidth.
  - **Test the performance of integrated frontends**: Integrated DAC/ADC and RF frontends in a single chipset in GF 22FDX are crucial for ensuring that high-frequency signals in the V-band can be efficiently converted and transmitted with low noise and distortion.
  - **Optimize energy consumption**: Another key objective is to design the transceiver with energy efficiency in mind. For this demonstrator, 26 pJ/bit is aimed which leads to reduce the power requirements both for infrastructure and mobile devices, crucial for sustainable and early adaptation of 6G networks.
  - **Prepare for future standards**: The V-band transceiver demonstrator provides insights into system-level challenges and solutions, aiding the development of future 6G standards.
- For the D-band, the objective is to integrate the developed 16-GHz DAC/ADCs and frontends, along with an antenna, onto a PCB and assess the overall system performance. The objective of the 6G transceiver demonstrator for the D-band (110-170 GHz) is to showcase the feasibility and performance of high-frequency communication systems capable of supporting ultrahigh data rates. Specifically, these demonstrators aim to:
  - **Achieve ultrabroadband communication**: By leveraging the D-band's wider available bandwidth, the goal is to enable data transmission up to 112 Gbps.
  - **Develop advanced RF frontends and DAC/ADCs**: Integrate high-performance RF circuits, data converters, and antennae to test and validate the performance of transceivers operating in the D-band, with a focus on ensuring minimal power consumption and robust signal quality. The overall aimed energy efficiency is 20 pJ/bit.
  - **Evaluate signal propagation and channel characteristics**: Since higher frequencies in the D-band have different propagation characteristics compared to lower bands, the D-band demonstrator shall be able to analyse signal behaviour, coverage, and network performance.
  - **Support future 6G applications**: The demonstrators aim to validate the ability of the D-band transceiver to support emerging 6G applications such as immersive AR/VR, ultralow latency communication, and massive machine-type communications.

By achieving these goals, the 6G transceiver demonstrator for the D-band will contribute to developing energy-efficient, cost-effective, and high-performance solutions for future communication networks.

2.3 State-of-the-art high-speed transceivers

The 57 GHz - 71 GHz frequency range is primarily used for millimetre-wave radar research, communication systems, including 5G networks, and other kinds of scientific research as well as next-generation industrial wireless applications and fixed wireless access. State-of-the-art transceivers in this frequency range are implemented using different technologies depending on the requirements of the targeted applications. Silicon-Germanium (SiGe) technology [1,2] has been widely adopted due to its excellent performance in terms of speed and integration capabilities as well as for its cost-effectiveness, in particular for automotive radar frontends. On the other hand, if ultimate output power capability is required, both gallium arsenide (GaAs) and gallium nitride (GaN) [1,3] devices are favoured for their high output power and efficiency, making them suitable for long-range communications. Whereas GaAs is a mature technology for this frequency range, GaN is still an emerging technology for applications in this part of the spectrum and thus adapted if ultimate output power from solid-state devices is required. Although being well established and providing excellent high-frequency operation with low noise figures, high gain, and moderate output power, indium phosphide (InP) technology in this frequency range is still too expensive for commercial high-volume applications.

State-of-the-art transceivers in the D-band provide data rates exceeding 10 Gbps. Nevertheless, achieving low power consumption at the same time as cost-effectiveness is critical. These metrics are very important for successful deployment in commercial, medium- and high-volume applications such as wireless communication. Hence, the challenges in this frequency range are to maintain signal integrity in particular during up-/down-conversion and transition between different chips and components. As a consequence, the integration of as many if not all components on a single chip while maintaining performance is important not only for cost effectiveness but also for reliable operation of high-bandwidth systems [4] at high frequencies. For this, CMOS technology provides the best platform [5].

The 110 GHz - 170 GHz frequency range is essential for advanced applications like high-capacity wireless backhaul, satellite communications, next-generation imaging systems, and high-capacity low-latency wireless communication systems such as 6G. Because of the propagation conditions and the performance of commercial semiconductor technologies in this frequency range, photonic technologies [6] relying on optical methods are being explored to achieve higher data rates above 100 GHz. In particular, silicon photonics offers promising results in terms of bandwidth and integration because it combines silicon electronics with photonics. However, it is questionable if such systems will be suited for mobile devices and if such systems will be competitive in price with full electronics systems, which have to achieve multigigabit data transmission rates (up to several tens of Gbps) while providing enhanced modulation schemes such as higher-order QAM (Quadrature Amplitude Modulation) to use the available spectrum efficiently. The design challenges above 100 GHz to be addressed are to provide sufficient output power in order to address the increased atmospheric absorption which can limit the effective operation range. For this SiGe BiCMOS technologies have been adapted [7], as GaN is not yet widely developed and available for this frequency range [8]. Finally, advanced CMOS technologies have already been explored for data-transmission systems above 100 GHz [9].

Both frequency ranges show significant advancements in transceiver technologies aimed at meeting the demands of modern communication systems. Ongoing research focuses on improving data rates, reducing power consumption, and overcoming physical limitations associated with higher frequencies.

3. Requirements and specifications

3.1 Performance requirements

Table 1 shows the key performance indicators of the proposed TRx architecture consisting of multiple sub-blocks such as analogue/mixed-signal components, including DACs and ADCs, and an analogue frontend operating in the V- and D-bands.

Table 1. Targeted KPIs by the end of FirstTo6G

	V-band solution	D-band solution
DAC/ADC		
Mod. Bandwidth	8 GHz	16 GHz
Power Consumption	1.0 W	2.0 W
Modulation	Up to 128-QAM	Up to 128-QAM
Data Rate	56 Gbps	112 Gbps
Nyquist Filtering	Yes	Yes
On-chip DSP	Yes	Yes
Technology	GF 22FDX	GF 22FDX
Chip Area	8 mm^2	16 mm^2
Frontend		
RF bandwidth	14 GHz (57-71 GHz)	45 GHz (130-175 GHz)
Noise Figure	5 dB incl TDD switch	<6 dB
Output power	10 dBm/ant. path @ -27dB EVM	> 0 dBm
Power consumption	100 mW/Tx ant. path in a multiantenna config, 300 mW & 200 mW for up- and down-converters, respectively	< 300 mW
Supported mod. bandwidth	8 GHz	>16 GHz
Technology	GF 22FDX	GF 22FDX/SiGe/GaAs
Overall System		
Mod. Bandwidth	8 GHz	16 GHz
Freq. Range	57–71 GHz	130-175 GHz
Data Rate	56 Gbps	112 Gbps
Energy Efficiency	26 pJ/bit	20 pJ/bit
Total power consumption	<1.5 W	<2.5 W
Integration	Single Chip (GF 22FDX)	Multiple Chips

3.2 Hardware requirements

The objective of the V-band demonstrator is to show single-chip integration in an advanced CMOS process with high performance. For this, the technology of GlobalFoundry GF 22nm FDSOI has been selected, as it allows the cointegration of the high-speed data converters with a high-performance millimetre-wave frontend. A broadband antenna will be designed on a suitable high-frequency PCB and interconnected with flip-chip bonding. The data will be transferred onto the chip through a high-speed interface in real-time from and to an FPGA platform capable of processing the targeted data rate. At least two of these setups will be used to demonstrate data transmission in the frequency range of 57-71 GHz. By varying the distance between the transmitter and receiver, the maximum data transmission as a function of the distance will be evaluated.

A similar scenario is envisaged for the D-band demonstrator, where the same FPGA platform and CMOS system will be used to feed the SiGe frontend. The interconnection will be done with bondwires utilising a high-performance low-loss PCB, which is also suitable for the integration of the broadband D-band antenna. In order to boost output power and thus increase the useable communication distance, a GaAs frontend will be included in a test scenario between the RF output of the SiGe chip and the broadband on-PCB antenna. All connections will be done by bondwires if possible. Alternatively, flip-chip assembly will be explored if the

performance of the bondwires will not be satisfactory. Flip-chip assembly is not the preferred interconnection option due to the higher cost associated with it.

Based on the assembled hardware different use cases and applications can be explored in the two frequency ranges.

3.3 Use cases and application scenarios

The 6G-TRx demonstrator in the V-band can span various high-speed, high-capacity, and low-latency applications. Here are some key scenarios:

1. **High-Bandwidth Wireless Communication**:
    a. **Fixed Wireless Access (FWA)**: V-band transceivers can deliver fiber-like speeds over wireless connections for urban and suburban areas. This is especially useful for last-mile connectivity where physical infrastructure is costly or impractical.
    b. **Mobile Backhaul**: In 6G networks, V-band transceivers will play a crucial role in providing high-capacity wireless backhaul for mobile networks, linking small cells to the core network and enhancing coverage.
2. **Augmented and Virtual Reality (AR/VR)**:
    a. V-band transceivers enable low-latency, ultrahigh-definition AR/VR experiences in real-time by supporting high data rate transmission and minimal delays.
3. **Autonomous Vehicles and Intelligent Transportation Systems**:
    a. V-band communication can support vehicle-to-everything (V2X) technologies, enabling fast data exchange between autonomous vehicles, traffic systems, and roadside infrastructure.
4. **Industrial IoT and Smart Manufacturing**:
    a. High-speed V-band transceivers can facilitate real-time control and monitoring of industrial processes, enabling Industry 4.0 applications such as robotics, automated factories, and smart logistics through ultrareliable low-latency communication (URLLC).
5. **High-Definition Video Streaming and 3D Holography**:
    a. 6G demonstrator in the V-band will enable ultrahigh-definition (8k/16k) video streaming and 3D holographic communications, which require massive bandwidth and low latency. This is applicable in areas like telemedicine, entertainment, and remote collaboration.
6. **Wireless Data Centres and Edge Computing**:
    a. V-band transceivers can be used to establish ultrahigh-speed wireless interconnects between data centres and edge computing nodes, allowing for efficient handling of large volumes of data with minimal latency.

By integrating 6G transceivers in the V-band, these use cases would allow for new possibilities in communication technology, providing the speed and capacity required for future digital ecosystems.

The 6G-TRx demonstrator in D-band (130-175 GHz) offers unique capabilities for future 6G networks due to its extremely wide available spectrum and potential for ultrahigh data rates. Use cases and application scenarios for a 6G-TRx demonstrator in the D-band can be focused on bandwidth-intensive and ultrareliable communication applications. Key scenarios include:

1. Terabit Wireless Communications

- **Wireless Backhaul for 6G**: The D-band can support terabit-per-second (Tbps) wireless backhaul links, essential for handling the vast data requirements of future 6G networks. This can connect small cells, massive MIMO systems, and high-density urban networks, ensuring high-speed and ultrareliable connectivity.
- **Data Centres and High-Speed Interconnects**: The D-band can be used for high-speed interconnects between servers and data centres, where ultrafast, short-range wireless links can enhance performance and reduce latency.

2. Extended Reality (XR) and Holographic Communications

- **AR/VR and Holographic Telepresence**: D-band TRx can enable immersive technologies like AR, VR, and holographic communications due to its ability to handle ultrahigh-definition video streams with minimal latency. This can revolutionize entertainment, education, and remote work, where real-time data exchange is critical.
- **3D Holographic Teleconferencing**: A step beyond traditional video calls, the D-band can facilitate real-time 3D holographic meetings, requiring high data rates to render full-resolution holograms.

3. Industrial Automation and Smart Factories

- **URLLC**: D-band TRx systems can support industrial automation by enabling real-time control of machinery and robotics in smart factories, where delays or interruptions can significantly affect production.

4. Autonomous Systems and V2X Communications

- **Autonomous Vehicles**: The D-band's ability to transmit large amounts of data quickly is ideal for V2X communication, which requires fast data exchanges between vehicles, roadside infrastructure, and control centres to ensure real-time decision-making.

5. High-Resolution Imaging and Sensing

- **Remote Sensing and Environmental Monitoring**: D-band transceivers can enable high-resolution imaging systems that are used for environmental monitoring, weather prediction, or even space exploration, where high-frequency signals can provide detailed and accurate data.
- **Security and Surveillance Systems**: The D-band's high frequency allows for advanced sensing applications, such as high-definition radar for security purposes or autonomous surveillance systems that require fast data processing.

6. Space and Satellite Communications

- **Intersatellite Links**: D-band technology is suited for high-speed communication between satellites in low-Earth orbit (LEO), medium-Earth orbit (MEO), or geostationary orbits (GEO), where terabit-level data rates are needed to transmit data for Earth observation or communication services.

7. Advanced Healthcare and Telemedicine

- **Remote Surgery and Medical Imaging**: With D-band transceivers, remote surgery can be performed with real-time video feeds and low-latency control, while high-resolution medical imaging can be transmitted for real-time analysis by doctors in different locations.
- **Remote Vital Signal Monitoring**: The D-band transceivers offer significant bandwidth that allows us to real-time and continuously monitor the vital signals, *e.g.* heartbeat and respiratory rate, of patients, infants, or elders remotely. Due to the wide bandwidth and high frequency leading to high resolution, more vital signals such as phonocardiography and multiple targets can be detected.

8. Smart Cities and IoT Networks

- **High-Capacity IoT Networks**: The D-band can support the high-capacity, ultralow latency requirements of smart cities, connecting thousands of IoT devices used for traffic management, smart grids, and urban monitoring.
- **Public Safety Networks**: In emergency response scenarios, the high data rates and reliability of D-band communication can be crucial for transmitting real-time data to support public safety operations.

9. High-speed chip-to-chip communication

- **Artificial intelligence (AI)/machine learning (ML):** The recent technological and architectural innovations have shifted the main bottleneck of current and future processors from computation to communication. In general, data sharing and synchronization between the different processing elements of a computing system are communication-driven mechanisms that, as indispensable as they are for the operation of such a system, throttle execution and severely limit its potential. Replacing fixed wired interconnects with flexibly reconfigurable wireless data transmission addresses the persistent communication bottleneck for such applications.

- **Neuromorphic computing:** Similarly to AI/ML, studies have shown that under certain circumstances the communication between the computing noes is the limiting factor. Also, here the flexibility offered by wireless communication and the high data rates available in the D-band over short distances is a potential performance booster in such applications.

These use cases leverage the D-band's ability to support ultrafast, low-latency, and high-capacity communication, positioning it as a critical enabler for future 6G technologies.

4. Demonstrator design and architecture

4.1 Architecture overview

4.1.1 Demonstrator setup for below 100 GHz

Figure 2 illustrates the overall development plan, detailing how each consortium partner contributes to the envisioned V-band solution. The complete demonstrator includes the V-band supported single TRx-IC mounted on the PCB with the antenna.

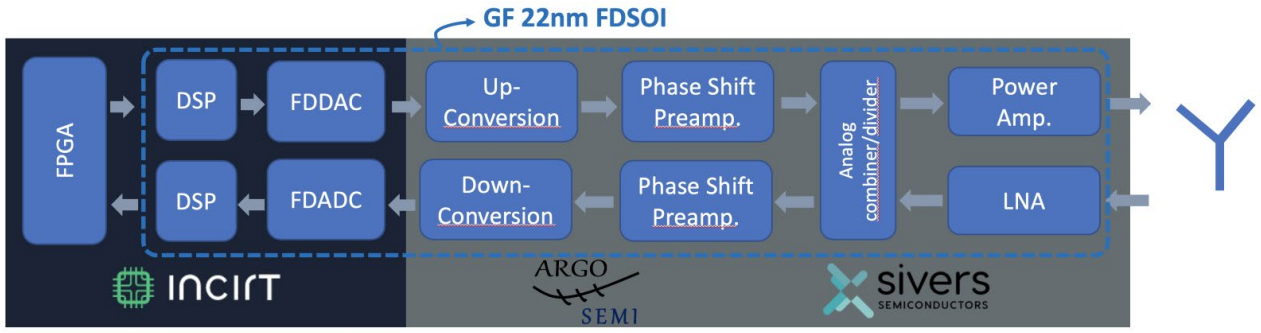

Figure 2. Overview of the targeted development and how the consortium partners contribute to the V-band solution

4.1.2 Demonstrator setup for above 100 GHz

Figure 3 presents a summary of the intended development and outlines the contributions of the consortium partners towards the D-band solution. The complete demonstrator includes the D-band-supported TRx-ICs mounted on the PCB with the antenna.

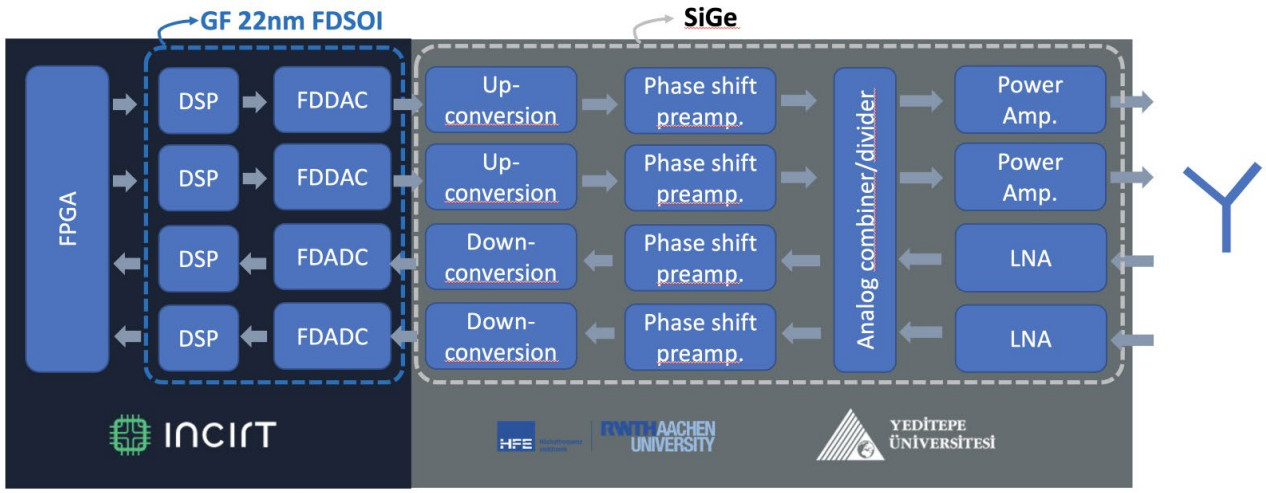

Figure 3. Overview of the targeted development and how the consortium partners contribute to the D-band solution

4.2 Key demonstrator components

The key components for the demonstrators will be developed by the project partners in the various WPs and eventually assembled for the two demonstrators. This requires coordination of the interfaces and final test results of the single components. This will be managed in regular meetings and determined by the tape-out dates and fabrication cycles of the chip manufacturers. The semiconductor technologies for the different building blocks have been defined, *i.e.* the V-band demonstrator will be based on a single chip in GF 22nm FDSOI from GlobalFoundries whereas the D-band frontend module chips will be designed in the G2 SiGe BiCMOS technology provided by IHP. GaAs frontends in a commercial III-V technology accessed through WIN semiconductor will be also assessed and designed within this project.

Suitable FPGA platforms capable of processing the targeted data rates are *e.g.* the Xilinx/AMD RFSOC ZR48DR with suitable interfaces, the HTG-960 Virtex UltraScale+ VU19P Development PlatForm, and the HTG-940 Virtex UltraScale+ QUAD FMC+ VU13P Development PlatForm both from HighTechGlobal. The availability of one of these or other suitable FPGAs within the consortium has to be identified. Alternatively, a suitable platform will be purchased and serve both the V- and D-band demonstrators.

In order to demonstrate the highest possible data transmission rate, advanced modulation techniques, and coding schemes will be evaluated on the hardware demonstrator platforms. Besides higher-order QAM, also more efficient amplitude phase shift keying (APSK) shall be assessed.

The antennae and phased antenna arrays will be designed on high-performance PCBs. Initial studies have shown that a rectangular patch antenna can cover the 130-175 GHz range with an estimated gain of 4-5 dBi. An alternative design which according to the literature can cover the targeted D-band frequency range is a broadband antipodal Vivaldi antenna.

Innovative baseband processing techniques will be developed to handle the demands of 6G and to be able to transmit and receive a large amount of data. Moreover, part of the data processing will also compensate for nonidealities of the hardware to maximise data throughput.

5. System-level assessment through simulations

The outcome of a detailed link budget analysis and architectural studies based on theoretical calculations and system performance evaluation has been reported in D1.1. This has led to the definition of a single up/down conversion architecture as the optimised system to address the requirements for the below-100 GHz applications. Based on these architectural studies D1.1. also specifies the performance of each building block. These specifications constitute the reference for evaluating the final demonstrator's performance. Hence, they are the input for the demonstrator definition.

On the other hand, D4.1 outlines the specification of the above-100-GHz Analogue Frontend and is thus the basis for the D-band demonstrator. D4.1 specifies the requirements of each sub-block based on system-level studies.

The performance metrics to which the validation of the final two demonstrators will be compared will be based on the abovementioned deliverables but might be adjusted to the performance measured after the first tape-outs. This is necessary to accommodate the knowledge acquired during the design and testing phase of the individual circuit blocks.

6. Demonstrator assembly and experimental setup

6.1 Demonstrator assembly

6.1.1 Below-100-GHz (V-band) demonstrator assembly

Referring to D1.1 for the details on the individual circuit blocks, simulation data, and link budget analysis, the proposed transceiver architecture for the below-100-GHz demonstrator is the single up-/down-conversion architecture detailed in Figure 4.

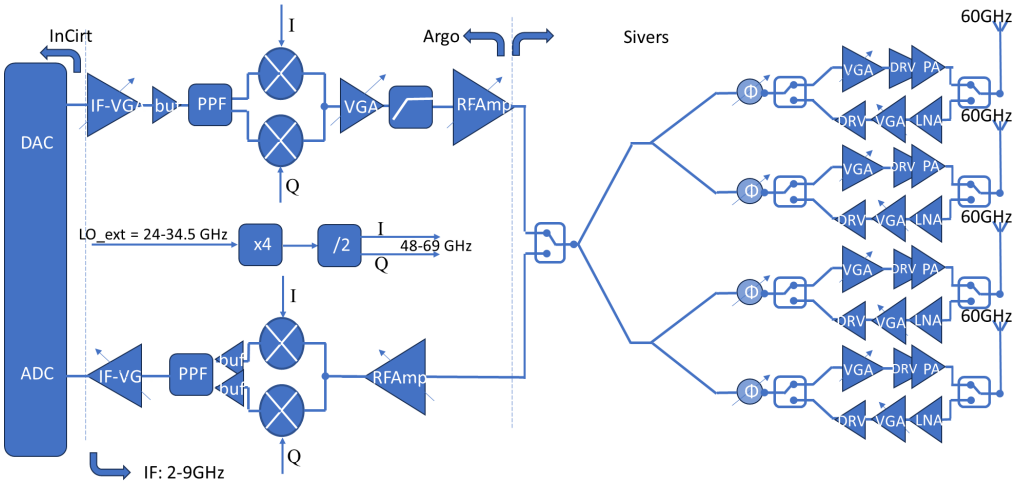

Figure 4. Proposed V-band TRx architecture (Source D1.1)

Since the V-band TRx will be mainly a fully integrated chip solution as defined in D1.1, for demonstrating purposes only the peripherals, *i.e.* the baseband digital frontend, the on-PCB antennas, and possibly a power management unit have to be added. The proposed overall integration and demonstrator setup is shown in Figure 5.

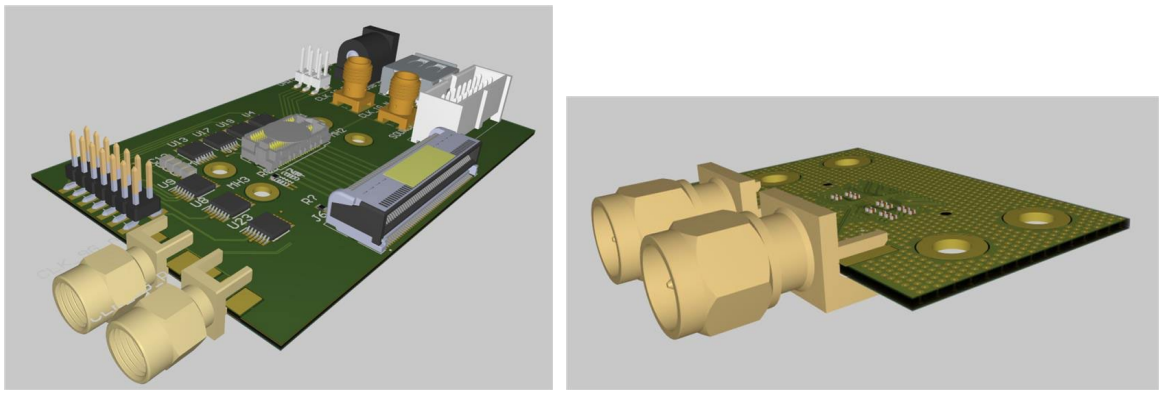

Figure 5. Example of anticipated V-band demonstrator board assembly based on the current version of InCirT's demonstrator boards Left: the mother/main board including high-speed interface connectivity, supply, clock, etc. Right: the carrier/daughter board with the IC flip chipped on it including differential analogue input and output.

The two main interfaces to be defined for the proposed assembly concept are the interface between the FPGA EvalBoard and the digital in- and outputs of the V-band TRx chip as well as the interface between the analogue output of the chip and the on-PCB antennae. For portability reasons, a power management unit (PMU) may be added to the PCB in order to provide all necessary supply voltages and currents out of a single DC source.

The interconnection between a suitable FPGA evaluation board and the V-band chip is required to guarantee the real-time transfer of the targeted data rate of up to 112 Gbps on both sides. Suitable FPGA platforms (Figure 6) serving as digital frontend for both the V- and D-band demonstrators are listed in Sec. 4.2. A possible connector is the CFP2 interface.

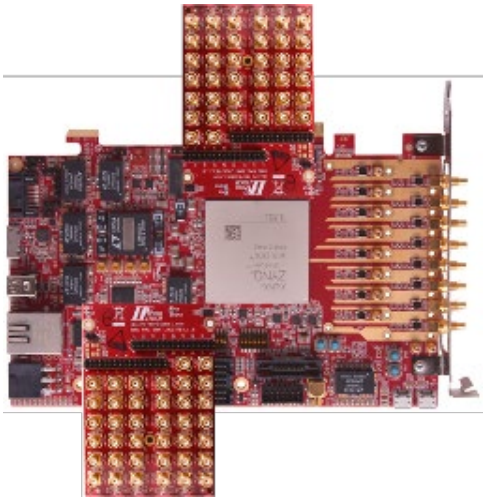

Figure 6. Example of suitable FPGA evaluation board as digital frontend

The connection of the V-band TRx chip with the on-PCB antennae will be established in the form of flip-chip bonding. This technique is suitable for this frequency range and allows a relatively low-loss interconnect of the 50-ohm on-chip power amplifier (PA) output and the input to the four antenna elements. The interface will be designed as coplanar waveguides (CPWs).

If necessary, a possible PMU line card for providing all necessary supply voltages will be interconnected with the board through a PCI Express connector similar to the one shown in Figure 7 developed by RWTH Aachen University and available for integration with the demonstrators. From the 18-V input voltage, the PMU can generate 6 constant voltages in the range from 0.6-5 V and 4 adjustable high voltages between 7 V and 12 V. If necessary, also two adjustable negative voltages can be supplied, in the case of III-V devices will be used in one of the demonstrators. The negative voltages are -4.5 V to 0 V. Moreover, 4 very low-voltage outputs in the range of 0-5 V with only a few milliamperes of bias currents. The negative voltages and the high voltages are coupled through a bias sequencer, which guarantees that III-V devices are biased in the correct order. The available PMU is controllable through a Teensy 4.1 microcontroller in combination with a Matlab graphical user interface (GUI).

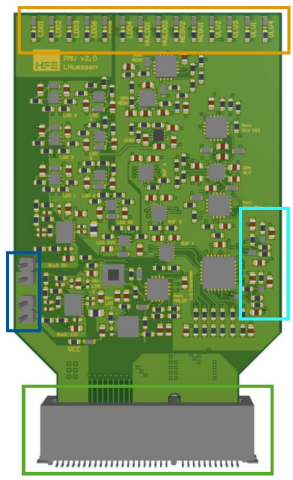

Figure 7. Example of power management unity assembly showing the connector interface

6.1.2 Above-100-GHz (D-band) demonstrator assembly

The above-100-GHz (D-band) demonstrator is defined in D4.1. The V-band system serves as input for the D-band demonstrator, which instead of antennae feeds the above-100-GHz SiGe chip through two 50-Ohm CPW inputs. The block diagramme of the above-100-GHz demonstrator is shown in Figure 8.

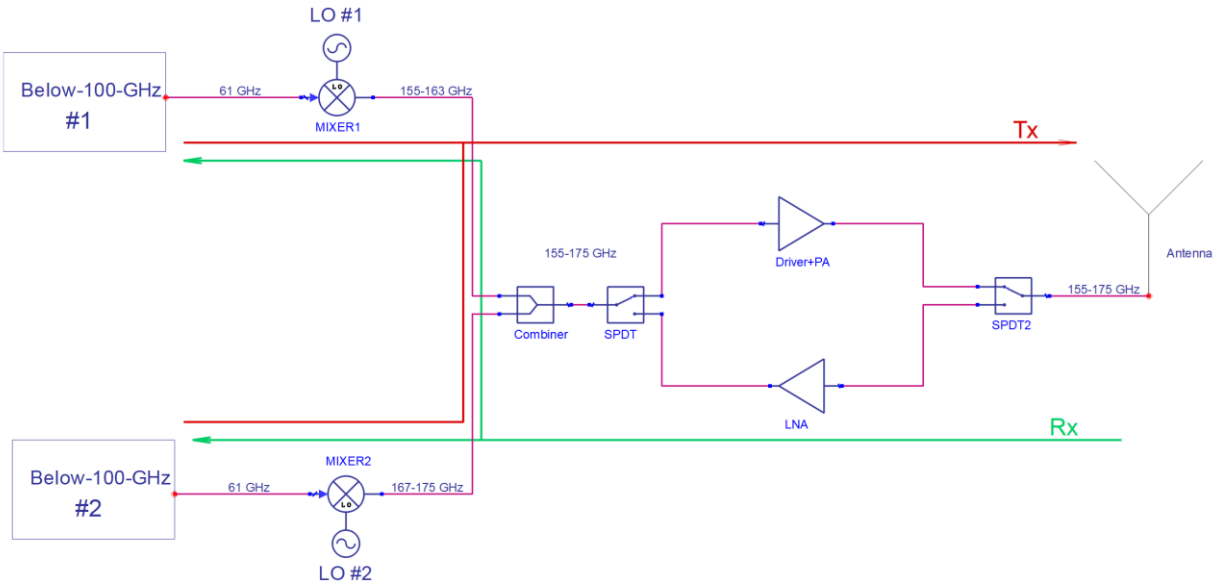

Figure 8. Block diagramme of the Above-100-GHz AFE (Source: D4.1)

Since the two LO signals will be generated on the SiGe chip, there are two interfaces besides the DC supply pins for the up-/down-conversion chip. As seen in Figure 8, two channels of the V-band demonstrator feed the two 50-Ohm inputs of the SiGe chip, which are directly connected to the bidirectional mixers. The chip-to-chip interconnection will be realised with bondwires, either directly from chip-to-chip or via the PCB. Electromagnetic simulations will determine which way will result in the most broadband interconnect providing at the same time a high degree of signal integrity. The output power of the V-band demonstrator will be adjusted through the inbuilt VGAs in order not to overdrive the passive mixers and thus reduce spurious signals at its output.

The high-frequency output of the chip is either connected directly through bondwires to an on-PCB broadband antenna or first connected to a GaAs analogue frontend (AFE) to boost the signal power before connecting to the antenna.

6.2 Physical testbed

In the test setup for the demonstrators, the signal generator implemented in the FPGA evaluation board emulates a user transmitting a high-data-rate signal with up to 8 GHz and 16 GHz of instantaneous bandwidth in the uplink direction. A MIMO 4×4 signal configuration can be supported for the below-100-GHz demonstration scenario. Noise or obstructions may be applied to simulate realistic radio channel conditions between the transmit and receive antennae. A second demonstrator assembly acts as the receiver in the final test setup, capturing the signal transmitted and then providing that as data via a real-time streaming interface to a personal computer. There, the signal is further processed utilising different receiver architectures and evaluated by comparing it with the original transmit data.

As part of the demonstration, the distance between the transmit antenna array and the receive antenna array is varied to determine the maximum link length. For the V-band demonstrator, also the alignment of the two modules will be varied in order to demonstrate and evaluate the beam-steering capabilities implemented into the chips.

The demonstrators will be tested in a controlled indoor environment and different channel impairments will be added to the direct link to simulate various realistic communication scenarios. These channel impairments can be metallic and nonmetalic shapes as well as absorbing materials in order to change the signal propagation between sender and receiver.

These 6G testbeds are flexible and scalable to address a multitude of frequency bands, frequency bandwidths, and waveform types. This flexibility allows us to tackle emerging 6G R&D testing challenges with up to 16 GHz of bandwidth in D-band (140-170 GHz) and 8 GHz in V-band (57-71 GHz).

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